

TITLE OF THE INVENTION

Semiconductor Device Including Voltage Conversion Circuit Having Temperature Dependency

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a semiconductor device including a voltage conversion circuit which converts the voltage value of an input voltage according to the change of the resistance value of a resistance section provided in a circuit as temperature changes and which outputs an
10 output voltage.

Description of the Background Art

Recently, as a portable device such as a cellular phone and a PDA (Personal Digital Assistant) spread widely, the quantities of information processed by these devices rapidly increase. Therefore, the capacity of a
15 work memory is greatly increased and a DRAM (Dynamic Random Access Memory) cell-based semiconductor memory is mainly employed as the work memory.

For the portable device driven by a battery, however, the increase of standby current due to a refresh operation which is essential to the DRAM
20 cell is considerably problematic.

Meanwhile, the data holding time of a DRAM cell is greatly influenced by operating temperature. As the operating temperature rises, the data holding time is shortened. It is therefore desirable to change the refresh interval of the DRAM cell as well as the temperature thereof so as
25 to conform to this characteristic.

Specifically, by controlling the refresh interval to become wider as temperature is lower, the refresh operation current of the DRAM cell at a temperature near a room temperature, at which the portable device is normally used, is lowered and the current consumption of the portable
30 device in a standby state is decreased.

Japanese Patent Laying-Open No. 9-204773 discloses a method for adjusting a current carried to a ring oscillator which serves as an oscillation circuit for setting a refresh interval according to temperature.

Conventionally, a voltage conversion circuit which supplies a constant voltage to the gate electrode of a transistor in the next stage so that the transistor in the next stage can carry a constant current, i.e., a circuit (hereinafter, referred to as "voltage conversion circuit") which
5 functionally converts the voltage value of an input voltage into a different voltage value and which outputs an output voltage has temperature dependency and changes the output voltage.

A current carried to the ring oscillator changes according to the change of this output voltage and the oscillation frequency of the ring
10 oscillator changes, accordingly.

However, it is known that the temperature dependency of the voltage conversion circuit disadvantageously becomes irregular due to the manufacturing irregularities such as the manufacturing irregularity of the resistance value of the resistance connected between a MOS transistor and
15 a power supply voltage line.

The irregular temperature dependency does not always occur in the same manner per wafer or per chip in a wafer plane.

SUMMARY OF THE INVENTION

The present invention has been achieved to solve the conventional
20 disadvantages. It is an object of the present invention to suppress a voltage conversion circuit having temperature dependency from being influenced by manufacturing irregularities.

It is another object of the present invention to attain a voltage conversion circuit having temperature dependency according to an
25 irregularity limitation requirement.

A semiconductor device according to an aspect of the present invention includes a voltage conversion circuit for converting a voltage value of an input voltage according to temperature change and outputting an output voltage, wherein the voltage conversion circuit includes: an input
30 section having a first transistor connected between a first voltage line and a first node, and carrying an input current by applying the input voltage to the first transistor; a current-mirror section having a second transistor connected between the first node and a second voltage line supplying a

different voltage from a voltage supplied by the first voltage line, and a third transistor connected between a second node, to which an output current according to the input current is carried, and the second voltage line, and forming a current-mirror by the second and third transistors; an
5 output section having a fourth transistor connected between the second node and the first voltage line, and outputting the output voltage according to the output current from the second node; and a resistance section connected only one of between the second voltage line and the second transistor and between the first voltage line and the fourth transistor, and
10 provided only as a resistance element in said voltage conversion circuit.

According to the present invention, as described above, the resistance section of the voltage conversion circuit is connected between the second transistor connected to the node through which the input current flows and the second voltage line or between the fourth transistor connected to the
15 node through which the output current flows and the first voltage line and the other resistance sections are not provided. It is therefore possible to determine the characteristic of converting an input voltage into an output voltage according to temperature change by the resistance value of the resistance section and the second transistor or by the resistance value of
20 the resistance section and the fourth transistor, and suppress the influence of manufacturing irregularities between the second and fourth transistors.

A semiconductor device according to another aspect of the present invention includes a plurality of voltage conversion circuits each outputting an output voltage according to an input voltage, wherein each of the voltage
25 conversion circuits includes: an input section connected to a first voltage line, receiving the input voltage, and carrying an input current; a current-mirror section connected to a second voltage line supplying a different voltage from a voltage supplied by the first voltage line, and supplying an output current according to the input current; an output section connected
30 to the first voltage line, and outputting the output voltage according to the output current; and a resistance section connected one of between the current-mirror section and the second voltage line and between the output section and the first voltage line, the plurality of voltage conversion circuits

are cascaded to each other to form a plurality of voltage conversion circuit stages, and circuits elements forming the voltage conversion circuits are equal in connection relationship among the stages and the output voltage of each voltage conversion circuit stage rise or fall according to temperature rise.

According to another invention, the voltage conversion circuits equal in the connection relationship of circuit elements are cascaded to each other to form voltage conversion circuit stages, and each stage includes a resistance section having a positive or negative temperature characteristic. It is therefore possible to eliminate irregularities caused by the difference in the connection relationship of circuit elements between the stages and to attain greater temperature characteristics as a whole.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a voltage conversion circuit according to a first embodiment of the present invention;

Fig. 2 shows characteristics of transistors according to the first embodiment of the present invention;

Fig. 3 is a pattern layout view of the voltage conversion circuit according to the first embodiment of the present invention;

Fig. 4 is a block diagram of a voltage conversion circuit according to a second embodiment of the present invention;

Fig. 5 is a block diagram of a voltage source circuit according to the second embodiment of the present invention;

Fig. 6 is a circuit diagram of a constant voltage source circuit according to the second embodiment of the present invention;

Fig. 7 is a circuit diagram of an output voltage generation circuit according to the second embodiment of the present invention;

Fig. 8 is a circuit diagram of a basic ring oscillator according to the second embodiment of the present invention;

Fig. 9 is a block diagram of a voltage source circuit according to a third embodiment of the present invention;

Fig. 10 is a pattern layout view of voltage conversion circuits according to the third embodiment of the present invention;

5 Fig. 11 is a block diagram of a voltage source circuit according to a fifth embodiment of the present invention;

Fig. 12 is a circuit diagram of an output voltage generation circuit according to the fifth embodiment of the present invention;

10 Fig. 13 is a circuit diagram of a voltage conversion circuit according to the fifth embodiment of the present invention;

Fig. 14 is a block diagram of a voltage source circuit according to a sixth embodiment of the present invention;

Fig. 15 is a circuit diagram of a voltage conversion circuit according to the sixth embodiment of the present invention;

15 Fig. 16 is a circuit diagram of a tuning code generation circuit according to the sixth embodiment of the present invention;

Fig. 17 is a block diagram of a voltage source circuit according to a seventh embodiment of the present invention;

20 Fig. 18 is a circuit diagram of a constant voltage source circuit according to the seventh embodiment of the present invention;

Fig. 19 is a block diagram of a voltage source circuit according to an eighth embodiment of the present invention;

Fig. 20 is a circuit diagram of a constant voltage source circuit according to the eighth embodiment of the present invention;

25 Fig. 21 is a block diagram of a voltage source circuit according to a ninth embodiment of the present invention;

Fig. 22 is a circuit diagram of a select circuit according to the ninth embodiment of the present invention;

30 Fig. 23 is a circuit diagram of a voltage conversion circuit according to the ninth embodiment of the present invention;

Fig. 24 is a circuit diagram of an output voltage generation circuit according to the ninth embodiment of the present invention;

Fig. 25 is a circuit diagram of a voltage conversion circuit according

to a tenth embodiment of the present invention; and

Fig. 26 is a circuit diagram of a voltage conversion circuit as a reference example.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 Although the present inventor has conventionally known that characteristic irregularities generate to a voltage conversion circuit, appropriate analysis has not been performed as to which part greatly influences the irregularities and how to suppress the irregularities not by a manufacturing method but by the circuit arrangement of the voltage
10 conversion circuit.

Fig. 26 is a voltage conversion circuit 101 which has been previously studied by the applicant as a reference example.

Voltage conversion circuit 101 is characterized by obtaining large temperature change characteristics by employing two resistances R_p and
15 R_n .

However, the following matters have been discovered as a result of the present analysis.

As resistance R_p connected to the source of a P-type MOS transistor MPA and resistance R_n connected to the source of an N-type MOS
20 transistor MNB, resistances made of different materials are employed in view of the facilitation of connection and the like.

However, the irregularities of resistance values between the different materials tend to increase.

It has been further discovered that the temperature change element
25 of an input current I_{pi} side is the S factors of P-type MOS transistors and that of an output current I_{po} side is the S factors of N-type MOS transistors and that the irregularities of the S factors between the N-type and P-type MOS transistors generate.

In the following embodiments, discovered circuits that suppress
30 irregularities in view of the above respects will be described.

First Embodiment

In Fig. 1, a voltage conversion circuit according to a first embodiment is formed of an input section INA which is connected to a ground line

serving as the first voltage line and to which an input voltage BIASL0 of voltage conversion circuit 1 is inputted, an output section OUTA which is connected to a ground line and which outputs an output voltage BIASL1 of voltage conversion circuit 1 according to input voltage BIASL0, a current-mirror section CUA which is connected to a Vcc line serving as the second voltage line and which changes an output current IR1 carried to output section OUTA according to an input current IL1 that is carried to input section INA according to input voltage BIASL0, and a resistance section which is connected between the Vcc line and current-mirror section CUA.

It is noted that output current IR1 and output voltage BIASL1 change as the resistance value of the resistance section changes according to temperature change.

In addition, when the changes of input and output currents are described, it is assumed that input and output voltages change according to the changes of the input and output currents, respectively. Conversely, when the changes of input and output voltages are described, it is assumed that input and output currents change according to the changes of the input and output voltages, respectively.

Next, the configuration of voltage conversion circuit 1 in the first embodiment will be described in detail.

In Fig. 1, in an N-type MOS transistor MN1 which forms input section INA serving as the first transistor, a drain serving as one of conductive ends is connected to a first node N1, a gate serving as a control terminal is connected to a node that inputs voltage conversion input voltage BIASL0, and a source serving as the other conductive end is connected to the ground line.

Current-mirror section CUA is formed of a P-type MOS transistor MP1 which serves as the second transistor and which is connected to first node N1 on an input current IL1 path, and a P-type MOS transistor MP2 which serves as the third transistor and which supplies output current IR1 to a second node N2.

In P-type MOS transistor MP1, a source serving as one of conductive ends is connected to a third node N3, and a gate serving as a control end

and a drain serving as the other conductive end are connected to first node N1.

In P-type MOS transistor MP2, a source serving as one of conductive ends is connected to the Vcc line, a gate serving as a control end is connected to first node N1, and a drain serving as the other conductive end is connected to second node N2 of voltage conversion circuit 1.

In an N-type MOS transistor MN2 which serves as the fourth transistor forming output section OUTA, a drain serving as one conductive end and a gate serving as a control end are connected to second node N2 from which output voltage BIASL1 is outputted, and a source serving as the other conductive end is connected to the ground line.

Finally, the resistance section is a resistance X in Fig. 1 and connected between the Vcc line and third node N3, i.e., between the Vcc line and current-mirror section CUA.

Voltage conversion circuit 1 is characterized in that resistance X which is the resistance section is provided only between third node N3 and the Vcc line and that no resistances are provided in the other parts of voltage conversion circuit 1.

In addition, a voltage applied to resistance X is, for example, at least not less than 1/20 times as high as a voltage indicated by the S factor of P-type MOS transistor MP1.

Since the S factor is normally between 60 mV/decade and 100 mV/decade, the voltage applied to resistance X is not less than 3 mV.

In other words, when input current IL1 is set at, for example, 1 μ A, the resistance value of resistance X is about not less than 3 k Ω .

Therefore, the resistance of the resistance section described in this embodiment is provided besides an ordinary parasitic resistance caused by an active region or contacts and applied to the source, drain or the like.

Further, the resistance value of resistance X changes according to temperature change. Depending on purposes, a resistance material having a positive temperature characteristic that the resistance value rises as the temperature rises or a resistance material having a negative temperature characteristic that the resistance value falls as the

temperature rises is selected as the material of resistance X.

Specifically, as the resistance material having the positive temperature characteristic, n-type polysilicon, an n-type diffused layer, a p-type diffused layer or the like can be used. When the temperature rises from a room temperature to 70 to 80°C, the resistance values of the n-type polysilicon, the n-type diffused layer and the p-type diffused layer rise by about 2 to 4%, 8 to 12% and 8 to 12%, respectively.

As the resistance material having the negative temperature characteristic, impurity-undoped silicon, germanium or the like can be used.

The operation of voltage conversion circuit 1 will next be described.

It is assumed herein that P-type MOS transistors MP1 and MP2 operate in a sub-threshold region. Therefore, even with a small change in the voltage between the source and gate of each P-type MOS transistor, a current carried thereto greatly changes.

In voltage conversion circuit 1, as the resistance value of resistance X changes according to temperature, the voltage V_{gsL} between the gate and the source of P-type MOS transistor MP1 shown in Fig. 1 (gate-source voltage V_{gsL}) changes.

Accordingly, the gate-source voltage V_{gsR} of P-type MOS transistor MP2 changes, and output current I_{R1} and output voltage $BIASL1$ are determined.

More specifically, in the resistance section which has the positive temperature characteristic, when temperature rises, then the resistance value of the resistance section rises, gate-source voltage V_{gsR} of P-type MOS transistor MP2 rises, output current I_{R1} increases and output voltage $BIASL1$ rises.

In the resistance section which has the negative temperature characteristic, when temperature rises, then the resistance value of the resistance section falls, gate-source voltage V_{gsR} of P-type MOS transistor MP2 falls, output current I_{R1} lowers and output voltage $BIASL1$ falls.

That is, in voltage conversion circuit 1, when input voltage $BIASL0$ is constant, the change of output voltage $BIASL0$ according to temperature is determined by the resistance value of resistance X and the

characteristics of P-type MOS transistors MP1 and MP2 in the sub-threshold region. Therefore, voltage conversion circuit 1 is superior to the voltage conversion circuit shown in Fig. 26 in which the resistances are provided in the source of the P-type MOS transistor and the source of the N-type MOS transistor, respectively, in that the influence of the irregularities of the S factors between the two MOS transistors is eliminated.

Furthermore, since one resistance and one resistance material are employed, the problem of irregularities between resistance materials does not arise.

The above-described qualification will next be described using mathematical expressions.

To be specific, expressions are obtained based on the relationship between input current IL1 and output current IR1.

It is assumed herein that the channel widths of P-type MOS transistors MP1 and MP2 are WL1 and WR1 ($WL1 > WR1$), respectively.

It is also assumed that the channel lengths of MP1 and MP2 are equal.

Based on the relationship between the gate-source voltages of MP1 and MP2 in Fig. 1, the following relational expression (1) is obtained.

$$V_{gsL}(IL1) + IL1 \times RL1 = V_{gsR}(IR1) \dots (1)$$

In expression (1), $V_{gsL}(IL1)$ indicates the gate-source voltage of MP1 when input current IL1 is carried, and $V_{gsR}(IR1)$ indicates the gate-source voltage of MP2 when output current IR1 is carried.

Referring to Fig. 2, the characteristics of MP1 and MP2 in the sub-threshold region will be described. In Fig. 2, the vertical axis indicates $\log(i)$ which is the common logarithm of the drain current I of an MOS transistor and the horizontal axis indicates a gate-source voltage Vgs.

It is assumed herein that the S factors of MP1 and MP2 are both S and that symbol I means an arbitrary current value in the sub-threshold region.

As is obvious from Fig. 2, at current I, the following relationship is satisfied.

$$V_{gsR}(I) - V_{gsL}(I) = S \times \log(WL1/WR1) \dots (2)$$

In addition, the following relationship is satisfied.

$$\log(IR1) - \log(IL1) = \{V_{gsL}(IR1) - V_{gsL}(IL1)\}/S \dots (3)$$

Next, when $I = IR1$ in expression (2) and expressions (1) to (3) are
 5 rearranged, then a relational expression (4) for the relationship between
 IL1 and IR1 is derived.

$$IR1 = (WR1/WL1) \times IL1 \times 10^{(IL1 \times RL1/S)} \dots (4)$$

Using expression (4), the temperature change quantity (temperature
 characteristic) $IR1(Tb)/IR1(Ta) = \Delta IR1$ of input current IR1 as temperature
 10 changes from Ta to Tb is given as an expression (5).

$$\Delta IR1 = \Delta IL1 \times 10^{[\alpha \times \{1 - \Delta S/(\Delta IL1 \times \Delta RL1)\}]} \dots (5)$$

In expression (5), $\Delta IL1$, ΔS and $\Delta RL1$ represent temperature change
 quantities, i.e., $\Delta IL1 = IL1(Tb)/IL1(Ta)$, $\Delta S = S(Tb)/S(Ta)$ and $\Delta RL1 =$
 $RL1(Tb)/RL1(Ta)$, respectively.

15 In addition, a factor α (hereinafter, referred to as “amplification
 factor”) satisfies the following expression.

$$\alpha = IL1(Tb) \times RL1(Tb)/S(Tb) \dots (6)$$

Amplification factor α is determined by a certain temperature of
 interest, i.e., temperature Tb, and the value of amplification factor α is
 20 obtained by dividing the voltage applied to the resistance by the S factor.

Based on expression (5), temperature change quantity $\Delta IR1$ of output
 current IR1 of voltage conversion circuit 1 satisfies the following
 relationship with temperature change quantity $\Delta IL1$ of input current IL1.

$$\Delta IR1/\Delta IL1 = 10^{[\alpha \times \{1 - \Delta S/(\Delta IL1 \times \Delta RL1)\}]} \dots (7)$$

25 From expression (7), the ratio of the temperature change of output
 current IR1 to the temperature change of input current IL1 can be obtained.

For example, when voltage conversion circuit 1 is used as the voltage
 conversion circuit of a refresh timer of DRAM, the output current of the
 voltage conversion circuit is desired to have a positive temperature
 30 characteristic, i.e., to have a characteristic that the output current rises as
 temperature rises. Therefore, it suffices to select the material of resistance
 X to satisfy $\Delta S/(\Delta IL1 \times \Delta RL1) < 1$ based on expression (7).

For example, when the material of resistance X is the well resistance

of an N well and $\alpha = 1$, $\Delta IL1 = 1.1$, $\Delta S = 1.2$ and $\Delta RL1 = 1.2$, then $\Delta IR1/\Delta IL1 = 1.23$ and $\Delta IR1 = 1.36$.

Thus, expression (7) demonstrates that the temperature change of the output current relative to the input current can be determined based on the temperature change of resistance X and the S factors of the P-type MOS transistors.

In expression (7), ΔS is the temperature change quantity in the P-type MOS transistor and is not influenced by the S factor of the other N-type MOS transistors. It is therefore possible to suppress the influence of the irregularities of the S factors between the P-type MOS transistors and the N-type MOS transistors.

Further, in the operation of voltage conversion circuit 1, it is only resistance X that is influenced by the temperature change, so that it is possible to suppress the influence of irregularities of resistances made of different materials.

Fig. 3 shows an example of the pattern layout of voltage conversion circuit 1 in this embodiment.

The pattern layout of Fig. 3 shows P-type MOS transistors MP1 and MP2, resistance X and the Vcc line shown in Fig. 1.

In Fig. 3, PD1 and PS1 denote a drain active region and a source active region of MP1 and PD2 and PS2 denote a drain active region and a source active region of MP2, respectively.

PGA1 and PGA2 denote gate electrodes of MP1 and MP2, respectively.

AR1 denotes a zigzag pattern forming resistance X, that is, the pattern of an active region forming the well resistance of an N well.

A wiring NL1 corresponds to node N1 and is connected to PS1, PGA1 and PGA2 through contacts CH3, CH4, CH9 and CH10.

A wiring NL2 corresponds to node N2 and is connected to PS2 through contacts CH5 and CH6.

A wiring NL3 corresponds to node N3 and is connected to PD1 and AR1 through contacts CH1, CH2 and CH11.

A wiring VccL1 is the Vcc line and connected to PD2 and AR1

through contacts CH7, CH8 and CH12.

As can be seen, Vcc line VccL1 is directly connected to PD2 which is the drain of P-type MOS transistor MP2 while Vcc line VccL1 is connected to PD1 which is the drain of P-type MOS transistor MP1 through AR1 which is resistance X.

Fig. 3 shows that channel widths WL11 and WR1 of P-type MOS transistors MP1 and MP2 are equal. As already described, when the channel width of P-type MOS transistor MP1 is set larger than that of P-type MOS transistor MP2, P-type MOS transistor MP1 may be constituted by arranging a plurality of transistor patterns TAA shown in Fig. 3 in parallel.

In that case, since the basic transistor pattern is the same, it is possible to set the characteristic of the transistor having a large channel width and that of the transistor having a small channel width equal.

Second Embodiment

In the second embodiment, a case where voltage conversion circuit 1 in the first embodiment is applied to a ring oscillator for the refresh timer of DRAM will be described.

Referring to Fig. 4, a basic ring oscillator 3 is controlled by an output voltage BIASS of a voltage source circuit 2, a transmission signal RCYC0 from basic ring oscillator 3 is multiplied by N by a multiplication circuit 4, and an oscillation frequency RCYC of the refresh timer is thereby determined.

Referring then to Fig. 5, voltage source circuit 2 includes a constant voltage source circuit 5, voltage conversion circuit 1 which inputs output voltage BIASL0 of constant voltage source circuit 5 and which is shown in the first embodiment, and an output voltage generation circuit 6 which inputs output voltage BIASL1 of voltage conversion circuit 1 and which outputs output voltage BIASS.

Constant voltage source circuit 5 is, for example, one shown in Fig. 6 which is normally referred to as a "Weak Inversion type" constant voltage source circuit which includes P-type MOS transistors MP12 and MP13 forming a current-mirror and operating in a sub-threshold region.

Since N-type MOS transistors MN12 and MN13 included in circuit 5 also form a current-mirror, constant voltage source circuit 5 is a positive feedback circuit and outputs BIASL0.

Output voltage generation circuit 6 is, for example, one shown in Fig. 7. Output voltage generation circuit 6 amplifies current by as much as the size of a P-type MOS transistor MP15 twice as large as that of a P-type MOS transistor MP14 (the size of P-type MOS transistor MP15 is $WR0/WL0$ times as large as the size of transistor MP14 when gate lengths of MP14 and MP15 are equal and gate widths thereof are $WR0$ and $WL0$, respectively) and outputs the amplified current as a voltage.

That is, the level of input voltage BIASL1 inputted to the gate of an N-type MOS transistor MN21 is converted and the level-converted voltage is output as output voltage BIASS from an N-type MOS transistor MN22 so that the voltage level is suited for a circuit operation in the next stage.

Normally, the transistors of output voltage generation circuit 6 are expected to operate at a higher voltage than a threshold voltage.

Referring to Fig. 8, basic ring oscillator 3 is basically formed of M (odd-numbered) inverters. An N-type MOS transistor which receives output voltage BIASS of voltage source circuit 2 is inserted into the pull-down side of each inverter, whereby charges are extracted from the output node of the inverter at a constant current $I_c(T)$ mirrored from output voltage generation circuit 6.

In other words, the driving capability of each inverter is controlled according to the change of voltage conversion circuit 1 and the oscillation frequency of output RCYC0 of basic ring oscillator 3 is determined.

Moreover, through multiplication circuit 4, oscillation frequency RCYC of the refresh timer is determined.

As described above, by employing voltage conversion circuit 1 in the first embodiment, it is possible to realize the refresh timer less influenced by manufacturing irregularities and excellent in temperature dependency.

Third Embodiment

In the first and second embodiments, an example of the use of one voltage conversion circuit has been described. When the temperature

dependency of the output voltage and output current of the voltage conversion circuit is to be increased but only the temperature change of one resistance X is utilized, the selection of the resistance material is limited by the restriction of manufacturing or the like. Therefore, the desired great temperature dependency cannot be sometimes attained.

Considering this, the third embodiment is intended to attain a voltage conversion circuit and a voltage source circuit capable of attaining greater temperature dependency.

Referring to Fig. 9, a voltage source circuit 21 according to the third embodiment is formed by cascading voltage conversion circuit 1 and a voltage conversion circuit 11 to thereby form voltage conversion circuit stages.

It is assumed herein that voltage conversion circuits 1 and 11 are equal to voltage conversion circuit 1 shown in Fig. 1.

By cascading voltage conversion circuits 1 and 11, two voltage conversion circuit stages are constituted, making it possible to attain a voltage conversion circuit having large temperature change even when one voltage conversion circuit stage cannot exhibit a sufficient temperature characteristic.

Next, voltage source circuit 21 will be described using mathematical expressions.

It is assumed that the input current of the second voltage conversion circuit stage is $IL2$, the output current thereof is $IR2$, the amplification factor thereof is β and the resistance value thereof is $RL2$ and that $IR1 = IL2$.

In this case, the following expression (8) is given as in the case of expression (5).

$$\Delta IR2 = \Delta IL2 \times 10^{[\beta \times \{1 - \Delta S / (\Delta IL2 \times \Delta RL2)\}]} \dots (8)$$

Further, when the relationship with the first stage is considered, expression (8) is transformed to the following expression (9).

$$\Delta IR2 = \Delta IR1 \times 10^{[\beta \times \{1 - \Delta S / (\Delta IR1 \times \Delta RL2)\}]} \dots (9)$$

Now, the change quantity of a current according to temperature change (temperature change quantity of a current) will be considered while

taking concrete numeric values as an example. In case of the first voltage conversion circuit stage shown in the first embodiment, when $\alpha = 1$, $\Delta IL1 = 1.1$ and $\Delta RL1 = 1.2$, $\Delta IR1 = 1.36$.

5 In this embodiment, by contrast, when $\beta = 1$, $\Delta S = 1.2$ and $\Delta RL2 = 1.2$, $\Delta IR2 = 2.50$.

As can be seen, while temperature change quantity $\Delta IR1$ of the output current of the first voltage conversion circuit stage is 1.36, temperature change quantity $\Delta IR2$ of the output current of the second voltage conversion circuit stage is 2.50, thus demonstrating that it is possible to increase the temperature change quantity of the output current.

Next, pattern layout will be described.

Fig. 10 shows the pattern of first stage of voltage conversion circuit 1 and that of the second stage of voltage conversion circuit 11.

10 The patterns of voltage conversion circuits 1 and 11 are equal to part of the pattern shown in Fig. 3.

In the pattern of voltage conversion circuit 11, PD21 and PS21 denote a drain active region and a source active region of a P-type MOS transistor and PGA21 denotes a gate electrode thereof.

20 AR2 denotes a zigzag pattern forming a resistance X2, i.e., the pattern of an active region forming the well resistance of an N well.

In order to increase the resistance value, the length of each pattern may be increased with the pattern width kept unchanged, i.e., a plurality of stages of zigzag patterns may be continuously provided.

25 A wiring NL21 is connected to PS21 through contacts CH23 and CH24.

A wiring NL23 is connected to PS21 and AR2 through contacts CH21, CH22 and CH20.

Wiring VccL1 is the Vcc line and connected to AR2 through contact CH31.

30 In Fig. 10, the transistors of voltage conversion circuits 1 and 11 are designed to be equal in pattern and resistance X of voltage conversion circuit 1 is designed to be equal to resistance X2 of voltage conversion circuit 11.

With this designing, it is possible to prevent generation of great irregularities even when manufacturing irregularities such as the irregularity of dimensions occur.

5 Further, since the resistances are particularly important elements, it is desirable that active region widths $W1$ and $W2$, lengths $L1$ and $L2$ of respective voltage conversion circuit stages are equal, respectively and active region distances $S1$ and $S2$ are equal in Fig. 10.

When some of them are to be set equal, it is most preferable to set the pattern widths, i.e., active region widths equal.

10 This is because the pattern widths are smaller than the other dimensions and considered to have the greatest irregularity, depending on manufacturing methods.

Nevertheless, a pattern having greater ordinality is more excellent in suppressing irregularities. It is therefore considered that the repetition of the same pattern can better suppress manufacturing irregularities.

Therefore, it is preferable to repeat the active region distances or pattern distances and the lengths of respective stages equally.

15 In an actual device, however, the pattern distances and lengths of the respective stages are not equal due to the restriction of patterns and manufacturing irregularities and it is considered that they vary by about 10%.

By setting the directions of the respective patterns equal between the circuits, it is possible to prevent the occurrence of the irregularities of resistance values due to the asymmetry of the active regions resulting from the ion injection angle.

25 In this embodiment, an example of cascading two voltage conversion circuit stages has been described. However, the number of stages is not limited to two but may be three or more.

30 Further, the resistance values of the respective voltage conversion circuits may be changed. In that case, it is preferable to change the lengths of resistance patterns (the number of zigzag pattern stages or the like) in the respective voltage conversion circuits while using the same resistance material and setting the pattern widths of the resistances equal.

It is thereby possible to change the output of each stage according to the resistance value while suppressing the temperature characteristic irregularities of the output voltages of the respective stages.

5 The voltage conversion circuits described in this embodiment are equal in the connection structures of the respective constituent elements of the respective stages. Therefore, the elements that determine the temperature change quantities of the output voltage and the output current are those shown in expressions (5) and (9).

10 That is, the temperature change quantities of the output voltage and output current are determined by input current I_{L1} of voltage conversion circuit 1 determined by output BIAS0 of constant voltage source circuit 5 and temperature change quantities ΔR_{L1} and ΔR_{L2} of the resistance values and the S factors of the P-type MOS transistors.

15 In this embodiment, as for the S factors, only the S factors of the MOS transistors of one conductive type, i.e., the P-type MOS transistors may be considered and the influence of the process irregularities of the S factors between the N-type MOS transistors and the P-type MOS transistors can be suppressed.

20 As for the resistance values, by using the same resistance material for resistances R_{L1} and R_{L2} , it is possible to eliminate the irregularity factors between the resistance materials and to suppress resistance irregularities.

The reasons that the resistance irregularities can be suppressed are considered as follows.

25 For example, when resistance materials A and B are used, the central resistance value of resistance material A and that of resistance B different from resistance material A are often shifted from expected values, respectively.

30 Therefore, when different resistance materials are used, great irregularities, to which the irregularities in materials and those between materials are added, sometimes generate.

When the same resistance material is used, the influence of the irregularity between the different materials can be eliminated.

By using a layout pattern common to the respective stages, it is possible to further suppress irregularities.

Conventionally, since irregularities increase as the number of circuits increases, it is not considered appropriate to increase the number of circuits.

However, as described in this embodiment, attention is paid to irregularities of the S factors and resistance materials between the MOS transistors among the irregularities, and the configuration of suppressing the irregularities is provided. With this structure, even when the number of circuits or stages increases, it is possible to suppress irregularities as a whole.

Further, as long as the requirements of the S factors and resistance materials are satisfied, it is considered that irregularities can be made within a certain range even when circuit configurations of the respective stages slightly differ.

As described above, according to the third embodiment, by cascading the voltage conversion circuits capable of suppressing the irregularities of S factors between the MOS transistors and the irregularities of resistances between the resistance materials, it is possible to attain great temperature characteristics while suppressing the manufacturing irregularities.

Further, according to the third embodiment, the temperature characteristics in a wide range can be realized according to the number of voltage conversion circuit stages. With this structure, BIASL0 that is the output of constant voltage circuit 5 shown in Fig. 5 and the input of voltage conversion circuit 1 is not required to have a large temperature change quantity.

Therefore, constant voltage source circuit 5 in this embodiment can also serve as a constant voltage circuit for an internal voltage generation circuit which generates the reference potential of a semiconductor device which does not require a large temperature change quantity. It can be thus expected to advantageously reduce layout area and decrease current consumption.

Since the constant voltage source circuit, in particular, is intended to

suppress the irregularities among the chips as much as possible, the layout area of this circuit itself tends to be very large. Therefore, it is greatly advantageous to be able to use the constant voltage source circuit as outputs to a plurality of circuits.

5 Fourth Embodiment

In the third embodiment, a case of suppressing both the irregularities of S factors among the transistors and those of resistance materials among the resistance sections has been described.

10 In a fourth embodiment, a case where the irregularities are not so suppressed, as compared with the third embodiment has been described.

In this embodiment, it suffices to suppress either the irregularities of S factors among the transistors or those of resistance materials among the resistance sections.

15 When it suffices to suppress the irregularities of S factors among the transistors, the same configuration as that shown in Figs. 9 and 10 may be considered. That is, one resistance section is provided in the same part of each stage and the first stage or voltage conversion circuit 1 and the second stage or voltage conversion circuit 11 use different materials for resistance X.

20 The configuration is advantageous in that pattern area can be reduced particularly when the resistance of the same resistance material cannot be used because of the layout limitation and the like.

25 When it suffices to suppress the irregularities of resistance materials among the resistance sections, voltage conversion circuits 101 shown in, for example, Fig. 26 may be cascaded.

In this case, the same resistance material is used for resistances R_p and R_n .

30 Further, even when the irregularities of S factors among the transistors and those of resistance materials among the resistance sections are both permitted, it is preferable that the equivalent circuits for cascaded voltage conversion circuits are equal among the respective stages.

Specifically, voltage conversion circuits 1 shown in Fig. 1 or voltage conversion circuits 101 shown in Fig. 26 may be cascaded.

When the equivalent circuits are equal in connection relationship of circuit constituent elements of the respective circuit stages, the tendencies of the irregularities become equal among the stages. Compared with a case of cascading circuits using equivalent circuits different among the stages, the irregularities can be made small and great temperature characteristics can be attained while suppressing the irregularities.

Further, by using a common pattern layout to the respective voltage conversion circuit stages, it is possible to suppress certain irregularities.

Moreover, as will be described later, by setting the resistance values of resistances R_p and R_n variable and adjustable, final irregularities may be suppressed.

It is preferable that the resistances employed in the respective stages have the same temperature characteristic, i.e., a positive temperature characteristic or a negative temperature characteristic.

When a voltage conversion circuit which includes a resistance having a positive temperature characteristic and a voltage conversion circuit which includes a resistance having a negative temperature characteristic are combined, for example, temperature that has risen is decreased, causing circuit pattern loss.

When a voltage conversion circuit which includes a resistance having a positive temperature characteristic and a voltage conversion circuit which includes a resistance having a negative temperature characteristic are combined, irregularities tend to increase and need to be suppressed.

As can be seen, according to the fourth embodiment, by setting at least the connection relationship of the circuit constituent elements of the respective voltage conversion circuit stages equal, it is possible to suppress irregularities which may be generated by the different connection relationship of the circuits. Even when a basic temperature change quantity per voltage conversion circuit stage is small, it is possible to eventually attain great temperature characteristics by cascading a plurality of such stages.

Further, by employing the resistance sections having the same positive or negative temperature characteristic in the respective stages, it is

possible to attain voltage conversion circuits having good area efficiency and good temperature characteristics.

Fifth Embodiment

5 In the third and fourth embodiments, the configuration of cascading a plurality of voltage conversion circuits formed of the same constituent elements has been described.

When different resistance materials are used for resistances X, there is a high probability that the absolute values of the resistances change without any correlation among them.

10 Even when the same resistance material is employed in the respective stages, slight irregularities may possibly generate.

Further, there is a probability that output BIASL0 of constant voltage source circuit 5 differs from expected output.

15 For example, when the absolute values of $IL1(Tb)$ and $RL1(Tb)$ greatly differ from expected values at temperature Tb in the configuration shown in Fig. 1, amplification factor α represented by expression (6) greatly changes, with the result that the temperature change quantity of the output current determined by expression (5) also greatly changes.

20 Taking them into consideration, the fifth embodiment is intended to control the temperature change quantity by providing a mechanism which can adjust circuit parameters.

It is assumed herein that the expected value of amplification factor α is 1 ($\alpha = 1$) and that the ratio of the gate widths or mirror ratio of P-type MOS transistors MP3 and MP4 is $WR1/WL1 = 1/10$.

25 Under these conditions, $IR1(Tb) = IL1(Tb)$ according to expressions (4) and (6).

Fig. 11 differs from Fig. 9 in that output BIASL0 of constant voltage source circuit 5 and output BIASL1 of the first stage of voltage conversion circuit 12 are both inputted to an output voltage generation circuit 61.

30 Referring to Fig. 12, output voltage generation circuit 61 in this embodiment differs from output voltage generation circuit 6 shown in Fig. 7 in that N-type MOS transistors MN14 to MN19 shown in Fig. 12 are provided and currents $IR0$, $IR1$ and $IR2$ can be selectively carried according

to adjustment test signals TMTUNE1 and TMTUNE2 which are select signals.

That is, in accordance with the adjustment test signals, one of the outputs of constant voltage source circuit 5, the first stage of voltage conversion circuit 12 and the second stage of voltage conversion circuit 13 shown in Fig. 11 is selected, and it is possible to check which output is selected from output BIASS of output voltage generation circuit 61.

In the normal operation, an output ZTUNE of logic circuit LG1 is "H"; therefore, IR2 is selected.

Referring to Fig. 13, voltage conversion circuit 12 differs from voltage conversion circuit 1 shown in Fig. 1 in that the resistance of the resistance section changes from resistance X to a variable resistance Z1, an adjustment mechanism is provided and the resistance value of the resistance can be varied. It is noted that the detail of variable resistance Z1 serving as the resistance section is given as an enlarged view shown in the upper part of Fig. 13.

More specifically, variable resistance Z1 is formed of four adjustment resistances (resistance values R0 to R3) having fuse elements F0 to F3 arranged in parallel and one fixed resistance (resistance value Rf).

Resistance values R0 to R3 are different, e.g., $R0 = 2 \times R1 = 4 \times R2 = 8 \times R3$. A final resistance value is determined by blowing the fuse elements F0 to F3 by laser trimming.

Alternatively, fuse elements F0 to F3 may be blown by a method other than the laser trimming.

In addition, voltage conversion circuit 13 shown in Fig. 11 is equal in configuration to voltage conversion circuit 1 shown in Fig. 1.

The resistance value adjustment sequence of voltage source circuit 22 in this embodiment will next be described.

The following two test modes for adjusting the temperature characteristic of voltage conversion circuit 12 are prepared and the resistance values are adjusted based on one of the test mode.

The first test mode is a test mode TM1 in which current IR0 of constant voltage source circuit 2 based on output BIASL0 of constant

voltage source circuit 2 can be monitored. In Fig. 12, the first test mode is set by setting adjustment test signals TMTUNE1 at "H" and TMTUNE2 at "L".

5 The second test mode is a test mode TM2 in which output current IR1 of voltage conversion circuit 12 based on output BIASL1 of constant voltage source circuit 12 can be monitored. In Fig. 12, the second test mode is set by setting adjustment test signals TMTUNE1 at "L" and TMTUNE2 at "H".

10 The outline of the adjustment sequence using these test modes is as follows. It is assumed that temperature is Tb.

<1> Voltage source circuit 12 enters test mode TM1, and output BIASS of output voltage generation circuit 61 is measured and, indirectly, a current Itmr is measured.

15 Alternatively, oscillation frequency RCYC of the refresh timer may be measured through basic ring oscillator 3 operating in response to output BIASS as described in the second embodiment.

It is assumed that current IR0 is made equal to input current IL1 of voltage conversion circuit 12 and that current Itmr is a value obtained by multiplying input current IL1 by mirror ratio WR0/WL0 (the gate width ratio of P-type MOS transistors MP14 and MP15 shown in Fig. 12).

20 <2> Voltage source circuit 12 leaves test mode TM1.

<3> Voltage source circuit 12 enters test mode TM2, and output BIASS of output voltage generation circuit 61 is measured and, indirectly, current Itmr is measured.

25 Similarly to <1>, oscillation frequency RCYC of the refresh timer may be measured.

Similarly to <1>, current Itmr is a value obtained by multiplying input current IR1 by mirror ratio WR0/WL0.

30 <4> When the above-described condition of $IR1(Tb) = IL1(Tb)$ is set, variable resistance Z1 of voltage conversion circuits 12 and 13 is adjusted so as to be equal or closest to the result of <1> based on the result of <3>.

As described above, by adjusting the resistance value of the resistance included in voltage conversion circuit 12, it is possible to provide

a voltage source circuit having stable temperature characteristic without the influence of process irregularities.

5 In this embodiment, an example in which only the first stage of voltage conversion circuit 12 employs the variable resistance has been described. Alternatively, the second voltage conversion circuit stage may also employ a variable resistance.

10 Further, according to this embodiment, since one output voltage generation circuit can check the output voltages of a plurality of voltage conversion circuits using the adjustment test signals serving as select signals, it is unnecessary to provide output voltage generation circuits for the respective voltage conversion circuits for tests.

15 That is, the output voltage generation circuit can monitor not only the output of the final voltage conversion circuit stage of a plurality of cascaded voltage conversion circuit stages but also the outputs of the other stages.

Sixth Embodiment

20 The adjustment mechanism shown in Fig. 13 is advantageously simple and easily adopted. However, it is required to estimate the change of current IR1 (which is also the output current of the first stage of voltage conversion circuit 12) corresponding to a combination of R0 to R3 somehow or other so as to determine a final combination.

25 In this embodiment, tuning (hereinafter, referred to as "pseudo-tuning") which enable measuring the change of current IR1 corresponding to the combination of resistances R0 to R3 is performed, whereby a configuration in which fuses can be blown is shown based on the result of tuning.

Fig. 14 shows a voltage source circuit 23 capable of adjusting the temperature characteristics of the voltage conversion circuits in this embodiment.

30 Referring to Fig. 14, voltage source circuit 23 in this embodiment differs from voltage source circuit 22 shown in Fig. 11 in that signal TMTUNE2 and pseudo-tuning code signals TMSIG<3>, TMSIG<2>, TMSIG<1> and TMSIG<0> (hereinafter, generically referred to as

"TMSIG<3:0>") are inputted to the first stage of a voltage conversion circuit 14.

It is noted that the second stage of a voltage conversion circuit 15 is equal to voltage conversion circuit 1 shown in Fig. 1.

5 The configuration of voltage conversion circuit 14 shown in Fig. 15 corresponds to that of voltage conversion circuit 12 shown in Fig. 13, i.e., a variable resistance Z2 is formed of four adjustment resistances (resistance values R0' to R3') having P-type MOS transistors MP7 to MP10 arranged in parallel and one fixed resistance (resistance value Rf).

10 The gates of transistors MP7 to MP10 receive output ZTC<3:0> of tuning code generation circuits 7, respectively.

Referring to Fig. 16, in each tuning code generation circuit 7, a P-type MOS transistor MP11 is set to have a higher driving capability than that of an N-type MOS transistor MN3.

15 Here, MN3 receives output BIASL0 of constant voltage source circuit 5 and a drain current is limited.

Due to this, in a normal operation in which no pseudo-tuning is performed, signal TUTUNE2 is set at "L", a node NF2 is set at "H". When fuse F4 shown in Fig. 16 is not blown, nodes NF0 and NF1 are at "H" and an output ZTC<n> is at "L".

20 Conversely, when fuse F4 is blown, nodes NF0 and NF1 are at "L" and output ZTC<n> is at "H".

When pseudo-tuning is performed, signal TMTUNE2 is set at "H", whereby output ZTC<n> is determined according to pseudo-tuning code signal TMSIG<n> for adjustment.

25 The configuration of tuning code generation circuit 7 will be described in more detail.

Since a fuse blowing step is not executed yet, node NF1 is at "H".

30 When signal TMSIG<n> is set at "L", then output ZTC<n> is set at "H", the corresponding P-type MOS transistor which is shown in Fig. 15 and the gate of which receives ZTC<n> is turned off and the corresponding resistance are used.

On the other hands, when signal TMSIG<n> is set at "H", then

output ZTC<n> is set at "L", the corresponding P-type MOS transistor the gate of which receives ZTC<n> is turned on and the both ends of the corresponding resistance short-circuited. Namely, the resistance is not used.

5 Next, the resistance value adjustment sequence of voltage conversion circuit 14 in this embodiment will be described.

 <1> Voltage conversion circuit 14 enters test mode TM1 and output BIASS of output voltage generation circuit 61 is measured and, indirectly, current Itmr is measured.

10 Alternatively, as described above, oscillation frequency RCYC of the refresh timer described in the second embodiment may be measured.

 It is assumed that current IR0 is made equal to input current IL1 of voltage conversion circuit 12 and that current Itmr is a value obtained by multiplying input current IL1 by mirror ratio WR0/WL0 (the gate width ratio of P-type MOS transistors MP14 and MP15 shown in Fig. 12).

15 <2> Voltage conversion circuit 14 leaves test mode TM1.

 <3> Voltage conversion circuit 14 enters test mode TM2.

 <4> Output BIASS of output voltage generation circuit 61 for all or part of the combination of TMSIG<3:0> is measured and, indirectly, current Itmr is measured.

20 Similarly to <1>, oscillation frequency RCYC of the refresh timer may be measured.

 Current Itmr is a value obtained by multiplying output current IR1 of voltage conversion circuit 14 by the same mirror ratio as that described in <1>.

25 <5> Pseudo-tuning code signals TMSIG<3:0> equal to or closest to the result of <1> are determined based on the result of <4>.

 Steps <3> to <5> in the resistance value adjustment sequence described above are for pseudo-tuning. By performing this pseudo-tuning, it is possible to obtain a combination of TMSIG<3:0> for realizing the most ideal resistance values.

30 Next, it is necessary to relate this combination with actual fuse blowing information.

Referring to Fig. 16, in the normal mode (TMTUNE2 = "L"), ZTC is at "H" when fuses are blown and ZTC is at "L" when fuses are not blown.

Therefore, considering the relationship between TMSIG and ZTC when TMTUNE2 is at "H" already described above, it is understood from the above-described resistance value adjustment that fuses should be blown when TMSIG<n> is at "L" and may not be blown when TMSIG<n> is at "H".

As can be seen, with the configurations shown in Figs. 14 to 16, output BIASS of output generation circuit 61 can be measured by switching the resistance value of the variable resistance provided in voltage conversion circuit 14 in a pseudo manner, so that it is possible to determine the final fuse blowing information more accurately.

In this embodiment, the first stage of voltage conversion circuit 14 is constituted so that the resistance value can be adjusted. As shown in Fig. 14, alternatively, not the first stage but the second stage of voltage conversion circuit 15 may be constituted so that the resistance value can be adjusted.

Further, both the first and second stages of voltage conversion circuits may be constituted so that the resistance values can be adjusted. By so forming, it is possible to make finer adjustment.

However, there are cases where the resistance value can be sufficiently adjusted only by so forming one of the voltage conversion circuit stages.

Furthermore, there are cases where when many adjustment parts are provided, the circuit becomes disadvantageously complicated and large in area.

In these cases, one of the voltage conversion circuits has a variable resistance. The voltage conversion circuit is preferably the voltage conversion circuit which inputs the output of constant voltage source circuit 2, i.e., voltage conversion circuit 14 in this embodiment.

The reason is as follows. The adjustment tends to be easier when the resistance value is adjusted in the first voltage conversion circuit stage before the irregularities are amplified than the resistance value is adjusted in the second stage after great irregularities in the first stage are amplified.

Seventh Embodiment

In the fifth embodiment, the temperature characteristic is adjusted by adjusting the resistance value of the resistance provided in the voltage conversion circuit.

5 In this embodiment, not the voltage conversion circuit but input BIASL0 of the first voltage conversion circuit stage is adjusted so that multiplication factor α becomes 1 at temperature T_b .

Referring to Fig. 17, a voltage source circuit 24 in the seventh embodiment is characterized in that a voltage adjustment circuit 8 is
10 provided between constant voltage source circuit 5 and voltage conversion circuit 1.

In the preceding embodiments, it is assumed that output current I_{R0} of constant voltage source circuit 5 is equal to input current I_{L1} of voltage conversion circuit 1. In this embodiment, by inserting voltage adjustment
15 circuit 8, output current I_{R0} of constant voltage source circuit 5 is not always equal to input current I_{L1} of voltage conversion circuit 1.

Voltage conversion circuit 1 is equal in configuration to that shown in Fig. 1 except that the input of circuit 1 is replaced from BIASL0 to BIASL00.

Referring to Fig. 18, in which the configuration of voltage adjustment
20 circuit 8 is shown, when $ZTC\langle n \rangle$ is inactive, an input current I_{L00} is determined by a P-type MOS transistor group PW0 and when one $ZTC\langle n \rangle$ is activated, one transistor of a P-type MOS transistor group PW1 consisting of transistors having different gate widths is activated, whereby
25 the gate width of the P-type MOS transistor is adjusted to make input current I_{L00} adjustable.

As can be seen, by adjusting the mirror ratio of voltage adjustment circuit 8 (the ratio of the sum of the gate widths of activated PW1 and PW0 to the gate width of PW2), output current I_{R00} and output BIASL00 are
30 determined.

The adjustment method in this embodiment is the same pseudo-tuning method as that described in the eighth embodiment and the adjustment sequence is the same as that described in the eighth

embodiment, as well.

In step <4> of the adjustment sequence shown in the sixth embodiment, in particular, pseudo-tuning code signals TMSIG<3:0> are sequentially changed and the mirror ratio of the input and output currents of voltage adjustment circuit 8 is changed to thereby obtain a mirror ratio under the condition that multiplication factor α becomes closest 1 at temperature T_b , i.e., the difference between $IL1(T_b)$ and $IR1(T_b)$ is minimized.

As described above, by adjusting the input of the voltage conversion circuit, it is possible to provide a voltage source circuit having stable temperature characteristic without the influence of process irregularities.

Eighth Embodiment

In the fifth to sixth embodiments, a case where the temperature characteristic of the voltage conversion circuit can be adjusted relative to processing irregularities has been described.

Normally, there is no correlation between the materials and the irregularities of the temperature characteristic of the resistance.

Therefore, when the resistance material of the resistance employed in the respective cascaded voltage conversion circuits differ, the temperature characteristic of the voltage conversion circuits cannot be managed to be a predetermined value as a whole without providing any adjustment mechanism for each resistance material.

When some resistance material is used in the constant voltage source circuit, it is also necessary to consider the resistance materials including that in the constant voltage source circuit.

Furthermore, since the adjustment mechanism adjusting the resistance value causes an increase in layout area, it is desirable that each adjustment target resistance is as low as possible.

Taking the above into consideration, this embodiment is provided.

Two types of resistance materials (A and B) are used in the constant voltage source circuit and the voltage conversion circuits. Among the circuits, only one voltage conversion circuit that uses resistance material A is employed and provided with a resistance adjustment mechanism while

the constant voltage source circuit and the other voltage conversion circuit(s) use resistance material B.

When the absolute value of resistance material A is determined according to the relationship with the absolute value of resistance material B of the constant voltage source circuit, then the relationship with the absolute value of resistance material B included in each of all the other voltage conversion circuits is automatically determined.

Referring to Fig. 19, which is a block diagram of a voltage source circuit 25 which embodies the above-described configuration, a constant voltage source circuit 51 and the second stage of a voltage conversion circuit 17 use resistance material B for resistances included therein. For brevity of description, it is assumed that the number of voltage conversion circuit stages is two.

Since constant voltage source circuit 51 and voltage conversion circuit 17 use the same resistance material, the resistance values thereof tend not to be greatly different, as compared with different resistance materials are used.

Further, the first stage of a voltage conversion circuit 16 uses resistance material A and includes a pseudo-tuning mechanism.

The second stage of voltage conversion circuit 17 is equal in configuration to voltage conversion circuit 1 shown in Fig. 1 except that resistance X is made of resistance material B.

Referring next to Fig. 20, constant voltage source circuit 51 in this embodiment is formed of a constant voltage section 52 and a startup section 9.

Constant voltage section 52 is equal to constant voltage source circuit 5 shown in Fig. 6 except that a resistance Y is made of resistance material B.

Startup section 9 is provided to be able to set the node NA of constant voltage section 52 at an operational stable point when power is turned on.

To be specific, when power is turned on, the potential of a node NB is raised by a P-type MOS transistor MP21. Accordingly, N-type MOS

transistor MN21 is turned on to thereby lower the potential of node NA.

When a power supply voltage is raised and the voltage becomes stably constant, then the voltage of node NB becomes not more than a threshold voltage and N-type MOS transistor MN21 is turned off to thereby stable the potential of node NA.

Next, the configuration of voltage source circuit 25 shown in Fig. 19 that is excellent in suppressing irregularities will be described based on mathematical expressions.

Output current IR0 of constant voltage source circuit 51 shown in Fig. 20 and the temperature change quantity of output current IR0 are obtained first.

When the mirror ratio of a current-mirror consisting of N-type MOS transistors NM12 and NM13 shown in Fig. 20 is 1:1, current IR0 is carried to P-type MOS transistors MP12 and MP13.

It is assumed herein that the channel widths of P-type MOS transistors MP12 and MP13 are WL0 and WR0 ($WL0 < WR0$) and that the channel lengths thereof are equal.

When the same relational expressions as expressions (1) and (2) are established to obtain IR0, the following relationship is satisfied.

$$IR0 = S \times \log(WR0/WL0)/RL0 \dots (10)$$

Further, the temperature change quantity $\Delta IR0$ of IR0 is assumed to be $IR0(Tb)/IR0(Ta)$ ($\Delta IR0 = IR0(Tb)/IR0(Ta)$), the following equation is deduced from expression (10).

$$\Delta IR0 = \Delta S/\Delta RL0 \dots (11)$$

Next, output current IR1 of voltage conversion circuit 16 shown in Fig. 19 and the temperature change quantity of IR1 are obtained.

When it is assumed that output current IR0 of constant voltage source circuit 51 is equal to input current IL1 of voltage conversion circuit 16 and expression (4) is assigned to expression (10), the following relationship is satisfied.

$$IR1 = (WR1/WL1) \times IR0 \times (WR0/WL0)^{(RL1/RL0)} \dots (12)$$

Further, when it is assumed that $WR1/WL1 = WR0/WR0$, the following relationship is deduced from expression (12).

$$IR1 = IR0 \times (WR0/WL0)^{((RL1/RL0) - 1)} \dots (13)$$

Temperature change quantity $\Delta IR1$ of output current $IR1$ is then obtained.

Since $IR0 = IL1$, $\Delta IR0 = \Delta IL0$.

5 When the above relationship and expression (11) are assigned to expression (5) about temperature change quantity $\Delta IR1$ of $IR1$, the following expression is obtained.

$$\Delta IR1 = \Delta IR0 * 10^{[\alpha * \{1 - \Delta RL0/\Delta RL1\}]} \dots (14)$$

10 As for amplification factor α , expression (4) is assigned to expression (6) while considering that $IR0 = IL0$, the following expression is obtained.

$$\alpha = \log(WR0/WL0) * \{RL1(Tb)/RL0(Tb)\} \dots (15)$$

When it is assumed herein that $RL1(Tb) = RL0(Tb)$ at temperature Tb , the following expression is obtained.

$$\alpha = \log(WR0/WL0) \dots (16)$$

15 When expression (16) is assigned to expression (14), the following expression is obtained.

$$\Delta IR1 = \Delta IR0 * (WR0/WL0)^{(1 - \Delta RL0/\Delta RL1)} \dots (17)$$

20 Expression (17) demonstrates that $\Delta IR0$, $\Delta RL0$ and $\Delta RL1$ are temperature constants determined by the resistance materials and it is, therefore, unnecessary to consider manufacturing irregularities.

In other words, by adjusting the resistance values so as to satisfy $RL1(Tb) = RL0(Tb)$ at temperature Tb as assumed above, it is possible to obtain the constant temperature change quantity of the output current from voltage conversion circuit 16.

25 In this embodiment, it suffices that the resistance value of resistance X of voltage conversion circuit 16 is set equal to that of resistance Y of constant voltage source circuit 51.

Likewise, output current $IR2$ of voltage conversion circuit 17 shown in Fig. 19 and the temperature change quantity of $IR2$ are obtained.

30 It is assumed herein that the input current of voltage conversion circuit 17 is $IL2$ and that the amplification factor of resistance material B used for the resistance of voltage conversion circuit 17 is β .

Under these conditions, amplification factor β is given by the

following expression similarly to expression (6).

$$\beta = IL2(Tb) \times RL2(Tb)/S(Tb) \dots (18)$$

Further, when it is assumed that $IR0 = IR1 = IL2$ at temperature Tb and S in expression (10) is assigned to expression (18), the following expression is obtained.

$$\beta = IL0(Tb) \times RL2(Tb)/S(Tb) = \log(WR0/WL0) \times \{RL2(Tb)/RL0(Tb)\} \dots (19)$$

In addition, $\Delta IR2$ is given by the following expression similarly to expression (5).

$$\Delta IR2 = \Delta IL2 \times 10^{[\beta \times \{1 - \Delta S/(\Delta IL2 \times \Delta RL2)\}]} \dots (20)$$

Amplification factor β includes a term $RL2(Tb)/RL0(Tb)$ included in expression (20) and in which the only absolute resistance value is shown.

However, since $RL0$ and $RL2$ are made of same resistance material B, the ratio thereof can be suppressed within irregularities in material.

Namely, the temperature change of output current $IR2$ of voltage conversion circuit 17 can be suppressed within irregularities of resistance material B.

As described above, since the irregularities between the resistances made of the same resistance material are small, the mechanism which corrects the process irregularities of the absolute value of resistance material B is less needed than a case of the resistance made of resistance material A.

Thus, the temperature change quantity of the output current of voltage conversion circuit 17 is obtained as described above. Therefore, even when the configuration shown in Fig. 19 is expanded to cascade voltage conversion circuits including a voltage conversion circuit using resistance material B, the temperature characteristics of the voltage conversion circuits merely depend on the ratio of the resistance value to $RL0(Tb)$ in each voltage conversion circuit at temperature Tb and the adjustment mechanism is less needed in the voltage conversion circuit including the resistance made of resistance material B.

As described above, the number of resistance materials used in the voltage conversion circuits in the voltage source circuit is limited to two or

less and the constant voltage source circuit and the voltage conversion circuits uses a common resistance material for the respective resistances, whereby it is possible to realize the configuration in which the adjustment mechanism is simplified.

5 In this embodiment, an example in which the first and second voltage conversion circuit stages use different resistance materials A and B, respectively, has been described. Alternatively, the constant voltage source circuit and the first and second voltage conversion circuit stages may use the same resistance material for the respective resistances.

10 Further, in this embodiment, a combination of constant voltage source circuit 51 shown in Fig. 20 and voltage conversion circuit 1 shown in Fig. 1 or the like exhibit a special advantage.

 In Figs. 20, 1 and the like, P-type MOS transistors operate in the sub-threshold region.

15 Due to this, the S factor dependencies of the respective circuits cancel one another, so that the dependency of the S factors on process irregularities is advantageously relaxed.

 Specifically, ΔS is included in the characteristic of the power of 10 in the temperature change quantity of the output current of the voltage conversion circuit as shown in expression (5). When the voltage conversion circuit is combined with the constant voltage source circuit shown in Fig. 20, ΔS and ΔS dependency in the front part satisfactorily cancel each other and the characteristic does not depend on ΔS .

20 Furthermore, the constant voltage source circuit and the voltage conversion circuit are similar in circuit configuration, so that it is possible to use a common layout pattern for the circuits and suppress manufacturing irregularities.

 Specifically, the layout pattern of voltage conversion circuit 1 shown in Fig. 10 corresponds to that of constant voltage source circuit 51 and the layout pattern of voltage conversion circuit 11 corresponds to that of voltage conversion circuit 17.

30 As for the resistances, it suffices to set $W1$ equal to $W2$, $S1$ equal to $S2$ and $L1$ equal to $L2$ in the resistance patterns.

When some of them are to be set equal, it is most preferable to set the pattern widths, i.e., active region widths equal.

It is also considered that the widths vary by about 10% due to irregularities or the like.

5 The number of zigzag patterns forming the resistance can be set different between constant voltage source circuit 51 and voltage conversion circuit 11.

It is also preferable that the transistor patterns of the respective circuits conform to each other as shown in Fig. 10.

10 The sizes such as the gate widths of the transistors may differ between the circuits. However, by assuming that basic pattern TAB of the transistors shown in Fig. 10 is one unit and arranging them in parallel to form a transistor having a large gate width, it is possible to suppress the irregularities between the transistor having a large gate width and the
15 transistor having a small gate width.

By setting the directions of the respective patterns equal between the circuits, it is possible to prevent the occurrence of the irregularities of resistance values due to the asymmetry of the active regions resulting from the ion injection angle.

20 In this embodiment, an example of making the patterns of constant voltage source circuit 51 and voltage conversion circuit 17 equal has been described. It is preferable to set the pattern of voltage conversion circuit 16 shown in, for example, Fig. 19, equal to those of constant voltage source circuit 51 and voltage conversion circuit 17.

25 That is, by setting the patterns of the respective stages equal, it is possible to more resist manufacturing irregularities.

The setting of transistor patterns equal described in this embodiment is also applicable to the other embodiments.

30 When the circuit configurations shown in the fourth embodiment are equal among the stages, it is particularly excellent in suppressing irregularities.

Ninth Embodiment

As described in the third embodiment and the like, it is possible to

generate a voltage and a current each having a large temperature change quantity by cascading a plurality of voltage conversion circuits.

5 In the ninth embodiment, an output branched in the course of cascade connection is used, whereby it is possible to selectively use voltages and currents having a plurality of different temperature change quantities.

Referring to Fig. 21, a voltage source circuit 26 in this embodiment is constituted, for example, that three voltage conversion circuits 18a to 18c are cascaded.

10 The configuration of voltage source circuit 26 shown in Fig. 21 differs from those of the voltage source circuits described above in that respective outputs BIASL0 to BIASL3 of constant voltage source circuit 5 and three voltage conversion circuits 18a to 18c are inputted to an output voltage generation circuit 62 and in that a select circuit 10 which selects whether to output BIASL0 to BIASL3 from the respective circuits is provided.

15 Referring to Fig. 22, select circuit 10 is formed of basic select circuits 10a to 10c corresponding to select signals ZSEL<1> to <3>, respectively.

Basic select circuits 10a to 10c are similar in configuration to tuning code generation circuit 7 shown in Fig. 16.

20 When fuse F5 is not blown, select signal ZSEL<n> is at "L" and the corresponding voltage conversion circuit is activated. When fuse F5 is blown, select signal ZSEL<n> is at "H" and the corresponding voltage conversion circuit is deactivated.

The correspondence of the selection of BIASL0 to BIASL3 to be input to output voltage generation circuit 62 and select signals is as follows.

25 Select BIASL0 : ZSEL<1> = "H", ZSEL<2> = "H" and ZSEL<3> = "H"
Select BIASL1 : ZSEL<1> = "L", ZSEL<2> = "H" and ZSEL<3> = "H"
Select BIASL2 : ZSEL<1> = "L", ZSEL<2> = "L" and ZSEL<3> = "H"
Select BIASL3 : ZSEL<1> = "L", ZSEL<2> = "L" and ZSEL<3> = "L"

30 Referring to Fig. 23, voltage conversion circuit 18a in this embodiment differs from voltage conversion circuit 1 shown in Fig. 1 in that an activation indication section 110 which receives the output of ZSEL<1> and determines whether to activate or deactivate the circuit is added.

ZSEL<1> is input to activation indication section 110 and voltage

conversion circuit 1 is controlled.

When ZSEL<1> is at "H", then the voltage of a node NC is fixed to a power supply voltage and that of a node ND is fixed to a ground voltage and output BIASL1 becomes "L".

5 When ZSEL<1> is at "L", nodes NC and ND are electrically disconnected from activation indication section 110 and the voltage is determined according to the operation of voltage conversion circuit 18a.

It is noted that voltage conversion circuits 18b and 18c are equal in configuration to voltage conversion circuit 18a.

10 Referring to Fig. 24, output voltage generation circuit 62 in this embodiment is constituted so that each of logic circuits LG2 to LG5 generates a signal SELm ($m = 0$ to 3) for selecting a predetermined output BIASLm in accordance with the correspondence between BIASL0 to BIASL3 and ZSEL<1> to ZSEL<3> described above.

15 The branch of BIASLm corresponding to SELm is selected and input current Itml of the circuit is determined.

A current obtained by multiplying input current Itml by mirror ratio WRo/WLo becomes output current Itmr and supplied, as output voltage BIASs, to the outside of the circuit.

20 As can be seen, one of the outputs of the constant voltage source circuit and the voltage conversion circuits that are cascaded is selected according to select signals, and the output voltage generation circuit generates an output voltage according to the selected output. Therefore, the voltage source circuit can select the voltage having the most
25 appropriate characteristic from among a plurality of voltages having different temperature change quantities and supply the selected voltage to the outside of the circuit.

30 That is, the output voltage generation circuit can utilize not only the output of the final stage of a plurality of cascaded voltage conversion circuit stages but also the outputs of the stages other than the final stage.

Tenth Embodiment

In the first to eighth embodiments, the voltage conversion circuit having the resistance provided between the source of P-type MOS

transistor MP1 and the Vcc line has been described.

As shown in Fig. 25, a voltage conversion circuit 19 having resistance X provided between a node N4 connected to the source of N-type MOS transistor MN2 and a ground line may be used.

5 That is, as shown in Fig. 25, a resistance section may be provided not between the Vcc line and a current-mirror section CUB but between an output section OUTB and the ground line.

In this case, N-type MOS transistors MN1 and MN2 operate in a sub-threshold region.

10 In addition, S factors for temperature characteristics are determined not by the P-type MOS transistors but by the N-type MOS transistors.

Normally, the S factor of an N-type MOS transistor is smaller than that of a P-type MOS transistor. When the resistances are equal, it is possible to increase the temperature change quantity of an output current or the like.

15 Besides voltage conversion circuit 19 shown in Fig. 25, the constant voltage source circuit may be realized by connecting the resistance to the source of the N-type MOS transistor.

20 In the embodiments described thus far, an example of MOS transistors has been described. Alternatively, MIS (Metal-Insulator-Semiconductor) transistors may be similarly used.

In the embodiments described thus far, an example in which the drain of P-type MOS transistor MP1 is directly connected to the drain of N-type MOS transistor MN1 and the drain of P-type MOS transistor MP2 is directly connected to the drain of N-type MOS transistor MN2 shown in Fig. 1 has been described. Alternatively, by the adjustment of the operation and the like, MIS transistors may be additionally provided between them, respectively.

30 Further, bipolar transistors may be used in place of MIS transistors. In this case, N-type MIS transistors are replaced by NPN bipolar transistors and P-type MIS transistors are replaced by PNP bipolar transistors.

Although the present invention has been described and illustrated in

detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.